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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/523,511	03/10/2000	Yasushi Kubota	49639(820)	4950

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EXAMINER
DINH, DUC Q

ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 12/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/523,511	KUBOTA ET AL.	
	Examiner	Art Unit	
	DUC Q DINH	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 1,5,12,14,16,18,20,22 and 24 is/are allowed.

6)☐ Claim(s) 2,3,6,11,13,15,17,19,21,23 and 25 is/are rejected.

7)☐ Claim(s) 4,7,8,9 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-25 in Paper No. 7 is acknowledged. Claims 1-25 are pending and presenting for examining

Claim Rejections - 35 USC § 112

2. Claims 8, 9 rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. For example, there is no disclosure of the claimed initialization circuit in the specification.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cairns et al. (U. P. Patent No. 6,266,041), hereinafter, Cairns

In reference to claim 2, Cairns discloses in Fig. 3 a data line driver circuit having a shift register consisting of a chain of master-slave flip-flops with both the master output and the slave output of each flip-flop being used to control the data line drivers, thus enabling the clocking rate of the shift register to be reduced. It is now common practice for the shift register of such a data line driver circuit to be composed of a chain of latches. Also, in order to minimize both the capacitative loading of the clock line or lines and the power consumption of the circuit, it is known to apply state-controlled clocking schemes to the shift register. For example U.S. Pat. No. 4,746,915 discloses a data line driver circuit comprising a first shift register which is split into smaller banks of DFF's or latches and a further shift register, operating at a lower frequency than the first shift register, which is used to selectively apply a clock signal to each bank of DFF's or latches. However, in all these circuit arrangements, it is only the flip-flop having its output at the `1` level and the flip-flop having a `1` at its input which require clocking in response to each clock pulse. FIG. 3 shows a data line driver circuit 20 in which the input and output of each DFF 21 is coupled to a respective input of an associated OR gate 22 which controls a pass gate 23 so as to ensure that only the required DFF's 21 are clocked by each clock pulse, as disclosed by T. Maekawa, Y. Nakayama, Y. Nakajima, M. Ino, H. Kaneko, M. Satoh and M. Kobayashi, `A 1.35-in.-diagonal wide-aspect-ratio poly-Si TFT LCD with 513 k pixels`, Journal, Pages 414-417, 1994 (col. 2, line 33 – 49).

It would have been obvious for one of ordinary skill in the art to provide the data line driver circuit comprising a first register which is split in smaller bank of DFF's or latches and a further shift register operating at a lower frequency than the first shift register which is used to selectively applied a clock signal to each bank of DFF's or latches.

5. Claims 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cairns as applied to claim2 above, and further in view of Ogawa (U. P. Patent No. 6,018,331).

In reference to claim 2, Cairns discloses the signals HSYNC is vary in accordance with the pulse signal transferred and a plurality of switching circuit 23 each connect and disconnect corresponding to the latch circuit to/from the clock signal line CL. However, Cairns fails to discloses in at least one part of a period in which the pulse signal is transferred from a first latch circuit through a last latch circuit, the clock signal has frequency lower than a normal operation mode. Ogawa discloses in FIG. 5A, which shows a block diagram of source driver 104, start pulse (DX) 202 is supplied to the shift input of shift register 204. This start pulse (DX) 202 is sequentially shifted within shift register 204 in accordance with shift clock (CLX) 201. This shift output is supplied to each individual AND gate 207 opened by enable signal 203. The output of each AND gate 207 is supplied to the source line 206 of each picture element 205. In addition, as discloses Fig. 8, in one part of the least one part of a period in which the pulse signal is transferred from a first latch circuit through a last latch circuit, the clock signal has frequency lower than a normal operation .

It would have been obvious for one of ordinary skill in the art at the time of the invention was made to applied the method of frame display control of Ogawa in the device discloses by Cairns for providing an image display device that when displaying image signals having a number of picture elements fewer than the number of picture elements in the image display device in the center of the display device, and displaying a frame around the periphery of the

displayed image, can display the frame adequately even in cases in which the input signals have a short horizontal blanking interval (col. 3, lines 10-15).

In reference to claim 6, Ogawa discloses the frequency difference as claimed

In reference to claims 11, Cairns discloses that as the shift register 51 is clocked by the clock signal CK, the state of each DFF 52 is passed to the next DFF along the register 51, and the effect of such clocking on the output C of the third DFF 52 from the left in the detail B is shown in the timing diagram of FIG. 7b, together with the clock signal CK and the horizontal synchronisation signal HSYNC. It will be appreciated that the output C incorporates a series of pulses of the duration of one period of the clock signal CK corresponding to each `1` level separated by gaps of three clock periods corresponding to the three consecutive `0` levels, as well as a pulse of two clock periods corresponding to the two consecutive `1` levels. The form of such an output C is particularly useful for controlling each line driver 54 as will be described in more detail below. Since such a circuit will tend to cause adjacent line drivers 54 to commence their operative cycle at data rate clock intervals, this will have the effect of smoothing the power dissipation of the circuit. As a result the circuit may bring about a reduction in the amount of voltage supply compensation and minimise switching interference on the data lines (col. 7, line 59 – col. 8, line 3).

In reference to claim 13, Cairns discloses in FIG. 4 shows the general architecture of a digital line-at-a-time data line driver circuit 30 which comprises an input register 31 to which digital video data is supplied in 6 or 8 bit RGB format, a storage register 32 in the form of digital latches, and digital-to-analogue converters 33 connected to the outputs of the storage register 32 and supplied with reference voltages for applying data to the data lines by way of output buffers

34. As the digital data bits are supplied to the input register 31, they are stored in the register 32 and, when a whole line of data has been stored, the contents of the input register 31 is transferred to the storage register 32 in order to control the D/A converters 33. In the case of small screen displays, the D/A converters may be connected directly to the data lines so as to charge the data lines by simple charge sharing, although output buffers are required for higher performance displays. Control logic 35 is provided for controlling the input register 31, the storage register 32, the D/A converters 33 and the buffers 34 on receipt of appropriate control signals (col. 3, lines 4-21).

In reference to claim 15, Cairns discloses that the drive circuit comprising clock means for generating a clock signal, a shift register comprising a chain of control shift elements having respective outputs, and a series of driver stages coupled to said outputs and controllable by control signals for sampling an input signal and for supplying the sampled signals to a corresponding series of lines, wherein each of the driver stages is associated with a respective one of the control shift elements and is locally controlled by a plurality of different control signals derived from signals generated by said one control shift element and/or at least one local control shift element in the vicinity of said one control shift element in the shift register in response to clocking of the shift register by the clock signal (col. 4, lines 12-26).

In reference to claims 17, 19, 21, Ogawa discloses an LCD having data driver and scan driver comprising a shift register circuit as claimed.

6. Claims 23 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cairns and Ogawa as applied to above claims, and further in view of Ino et al. (U. P. Patent No. 5,903,014), hereinafter.

In reference to claims 23 and 25, Cairns and Ogawa fail to disclose the process to form the data driver. Ino discloses that semiconductor devices each having integrated thin film transistors and the like are particularly suitable for driving substrates of active matrix type electro-optical devices, and therefore, they are being extensively developed at present. A thin film transistor has a semiconducting thin film as an active layer, which is made from amorphous silicon or polycrystalline silicon. The polycrystalline silicon transistor is superior in electric characteristics such as a carrier mobility to the amorphous silicon transistor, and it can be used for a peripheral driving circuit as well as for a switching element. In this regard, studies are being actively conducted on the polycrystalline transistors. On the other hand, when used for an active matrix display which is one example of the active matrix type electro-optical devices, the semiconductor device must adopt an inexpensive large-sized insulating substrate. From this viewpoint, there is a strong demand to develop a low temperature process capable of forming thin film transistors at a temperature in a range of 600.degree. C. or less, preferably, 400.degree. C. or less. Laser annealing or ion doping becomes important for the low temperature process. Moreover, from the standpoint of the structure, the thin film transistor is classified into a bottom-gate type (reversely staggered type) and a top-gate type. The bottom-gate type is superior to the top-gate type in terms of compatibility with the low temperature process, which has been proposed, for example, in Japanese Patent Laid-open Nos. Hei 4-186735 and Hei 6-350089.

It would have been obvious to use the process to produce the thin film transistor disclosed by Ino to make the data driver in the device of Cairns and Ogawa because it would provide the polycrystalline silicon transistor is superior in electric characteristics such as a carrier mobility to the amorphous silicon transistor, and it can be used for a peripheral driving circuit as well as for a switching element.

Allowable Subject Matter

7. Claims 1, 5, 10,12, 14, 16, 18, 20, 22, 24, are allowed.

8. Claims 8-9 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, first paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

9. Claims 4, 7, objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: none of the cited prior art teaches or suggest a shift register in which "in at least one part of the period in which the pulse signal is transferred from a first latch circuit to a last latch circuit,, the clock signal has a frequency which is lower than in a normal operation period and which gradually increases".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **DUC Q DINH** whose telephone number is **(703) 306-5412** The examiner can normally be reached on Mon-Fri from 8:00.AM-4:00.PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **RICHARD A HJERPE** can be reached on **(703) 305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

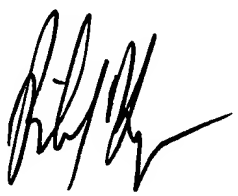
(703) 872-9314 (for Technology Center 2600 only)

Hand-delivery response should be brought to: Crystal Park II, 2121 Crystal Drive, Arlington, Va Sixth Floor (Receptionist)

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

DUC Q DINH
Examiner
Art Unit 2674

DQD
December 11, 2002



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SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600